

INTERIOR INT

DISCLOSURES

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors.

Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

For more information go to www.intel.com/benchmarks.

Performance results are based on testing as of several dates following result information and may not reflect all publicly available security updates. See configuration disclosure for details. No product or component can be absolutely secure.

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INTEL[®] EXPERIENCE DAY

СЕРВЕРНЫЕ ПРОДУКТЫ INTEL

Vasily . Lizunov @ intel . com

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CLOUDIFICATION EXPANSION AND SCALE TO THE POINT OF USE

DATA-CENTRIC ERA

DELIVER NEW SERVICES FASTER TO HANDLE THE DELUGE OF DATA

DELIVER OPERATIONAL EFFICIENCIES

DELIVER SECURE INFRASTRUCTURE TO PROTECT DATA PRIVACY

ENTERPRISE

CLOUD

DATA CENTER GROUP

INTEL.COM/XEONSCALABLE

IORE THAN

OF WORLD'S DATA WAS CREATED IN THE PAST TWO YEARS

AND ONLY

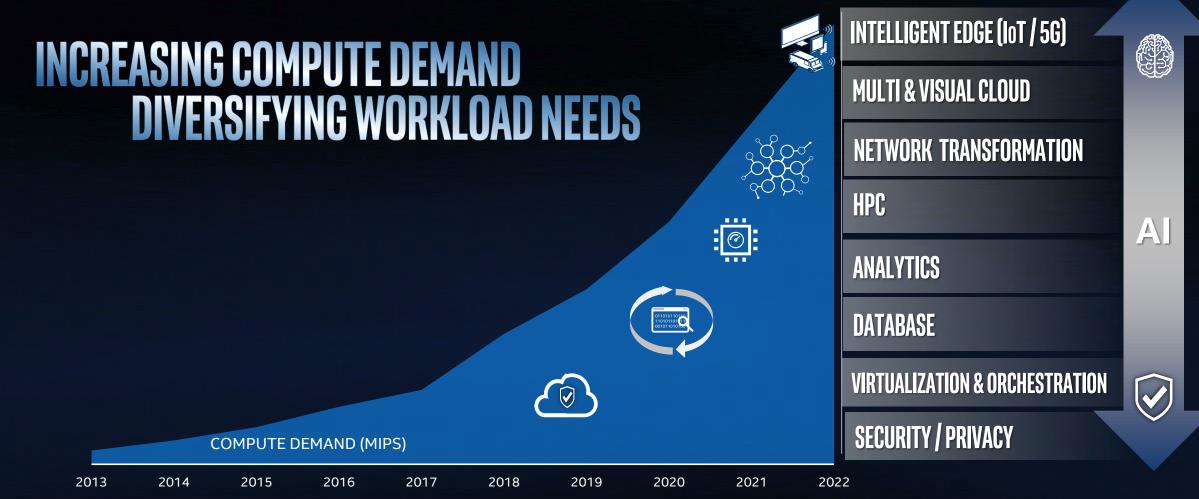
ANALYZED

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rom IDC Global DataSphere, Nov 2018



DRIVING BUSINESS TRANSFORMATION



Source: Intel analysis

∕intel

DATA-CENTRIC INFRASTRUCTURE FOCUS

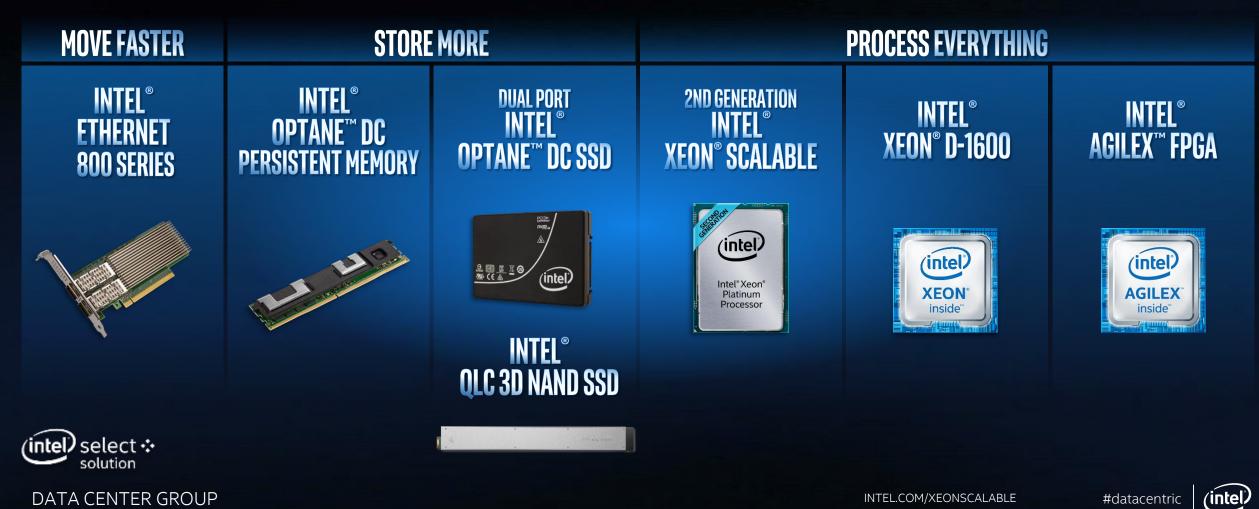


SOFTWARE & SYSTEM-LEVEL OPTIMIZED



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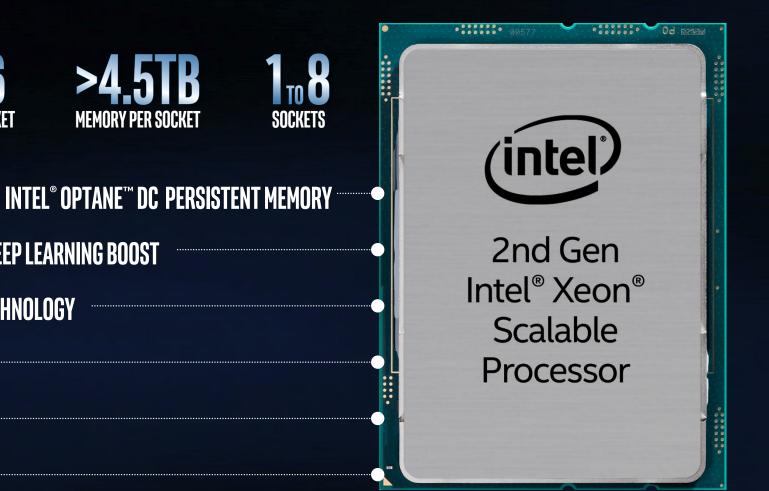
ANNOUNCED ON APRIL 2, 2019 2019 DATA-CENTRIC PORTFOLIO



DATA CENTER GROUP



SECOND GENERATION INTEL® XEON® SCALABLE PROCESSORS



SECURITY MITIGATIONS

CUSTOM SKUS

CLOUD-OPTIMIZED SKUS

CORES PER SOCKET

INTEL[®] SPEED SELECT TECHNOLOGY

NETWORK-OPTIMIZED SKUS

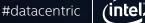
INTEL[®] DEEP LEARNING BOOST

BUILDING ON 20 YEARS OF DATA CENTER PROCESSOR INNOVATION

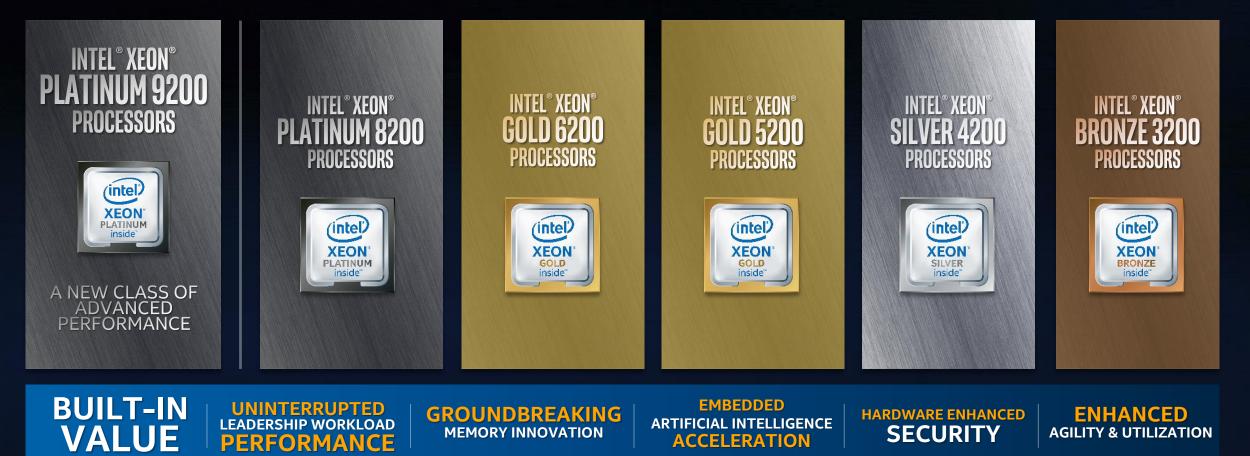
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STANDARD SKUS

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INTRODUCING SECOND GENERATION INTEL® XEON® SCALABLE PROCESSORS



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(intel)

INTEL[®] XEON[®] SCALABLE Platform & Processor Roadmap

2019	2020		2021	
PURLEY PLATFORM	WHITLEY PLATFORM (2 SOCKET)		EAGLE STREAM PLATFORM	
	COOPER LAKE	ICE LAKE		
CASCADE LAKE (+ EXTENDED REFRESH)			SAPPHIRE RAPIDS	
	CEDAR ISLAND PLATFO			
	COOPE			

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INTEL® XEON® D-1600 PROCESSOR INTEL® QUICKASSIST TECHNOLOGY | INTEL® ETHERNET | INTEL® VIRTUALIZATION TECHNOLOGY

COMPUTE

#1.29X MORE

INTEGER THROUGHPUT

NETWORK

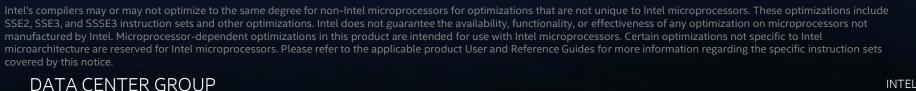
UP 1.25X MORE PACKET FORWARDING²

STORAGE

HP 2.7X LOWER

#1.4X HIGHER

READ/WRITE THROUGHPUT³





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INTEL.COM/XEOND



INTEL OFFERS A PORTFOLIO OF PRODUCTS FOR ADVANCED DATA-CENTRIC INTELLIGENCE











INTEL® XEON® SCALABLE PROCESSOR Best Performance, most scalable

DESIGNED FOR TRADITIONAL OPERATING ENVIRONMENTS WITH FLEXIBLE OPERATING SPACE AND POWER

(intel) XEON^{*} inside^{**}

INTEL[®] XEON[®] D PROCESSOR Optimized for density, lower power

DESIGNED FOR ENVIRONMENTS CONSTRAINED BY OPERATING SPACE AND POWER



INTEL ATOM® C PROCESSOR Purpose-built for very low power

DESIGNED FOR ENVIRONMENTS CONSTRAINED BY PHYSICAL SIZE AND EXTREME TEMPERATURES



INTEL® XEON® E PROCESSOR ENTRY SERVERS & EDGE APPLIANCES

DESIGNED FOR TRADITIONAL OPERATING ENVIRONMENTS AND SMALL BUSINESS CUSTOMERS



INTEL ATOM[®] C3000 PROCESSOR LANDSCAPE

Base Stations	Routers & Switches	Storage	Security	Web Servicing	Internet of Things
4G/5G base stations delivering SDN and NVF to the network edge	Low power, intelligent routers and switches supporting SDN and NFV	Energy efficient entry storage, entry SAN/NAS, and cold storage	VPN, firewall, ADC, IPsec and WAN acceleration appliances	Dedicated static web hosting and memory caching appliances	Low power intelligence at the edge from smart buildings, industrial IoT and more

(intel

Tremont: Top-level Design Targets

Single thread performance Networking

- Performance/mW
- Performance/mm²
- New instructions

Battery life

Performance/mW



Summary

- Tremont: Intel's next generation low power x86 microarchitecture
- Advancements on ISA, microarchitecture, security, and power management

Instruction Cache

Instruction Data

RS

- Out of order front end and 10 wide execution port back-end
- Significant IPC improvement vs. prior Intel low power x86 architectures
- Targeting a wide variety of products across client, data center, 5G networking and Internet of Things



DELIVERING DATA-CENTRIC PLATFORM LEADERSHIP

OVER 20 YEARS OF INTEL[®] XEON[®] PLATFORM LEADERSHIP

OS, SOFTWARE, WORKLOADS AND SERVICES	(intel) LIBRARIES AND FRAMEWORKS (intel) ENABLING AND SUPPORT (intel) select .
FIRMWARE AND DRIVERS	(intel) SOFTWARE (intel) DRIVERS (intel) FIRMWARE
CONNECTIVITY	(Intel) ETHERNET (Intel) OMNI-PATH FABRIC (Intel) SILICON PHOTONICS
MEMORY AND STORAGE	(intel OPTANE DC) (intel OPTANE
ACCELERATORS	E FPGAS NNPS (Intel) QUICKASSIST (Intel) GRAPHICS
PROCESSORS AND PLATFORMS	INTERING INTERIOR INTERIORI INTERI

END-TO-END PLATFORM INNOVATIONS TO DELIVER UNPRECEDENTED SCALE AND UTILIZATION

NOT A COMPREHENSIVE LIST OF PRODUCTS AND CAPABILITIES DATES, DETAILS AND INFORMATION ARE SUBJECT TO CHANGE WITHOUT NOTICE

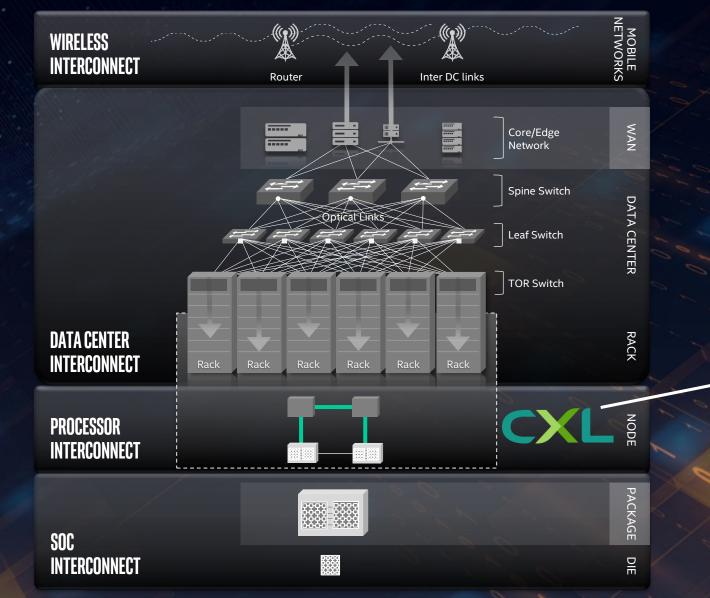
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PROCESSOR INTERCONNECT



INTERCONNECT DAY

APRIL 2019

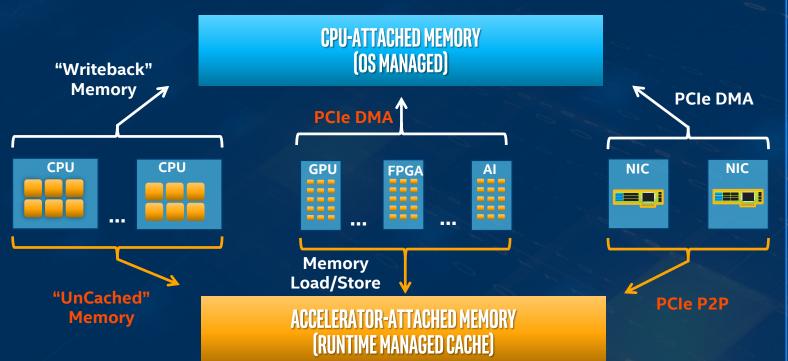
(intel)

CXL: A NEW CLASS OF INTERCONNECT FOR DEVICE CONNECTIVITY

WHY A NEW CLASS OF INTERCONNECT?

MOVE PAST THE PCIE LIMITERS ON HETEROGENEOUS COMPUTING AND SERVER DISAGGREGATION USAGES

- PCIe creates isolated memory pools with an inefficient mishmash of access mechanisms.
- Moving operands and results back and forth between accelerators and devices is painful and inefficient
- Resource sharing is all but disallowed.
- Latencies are an order of magnitude off of what is needed to enable disaggregated memory.



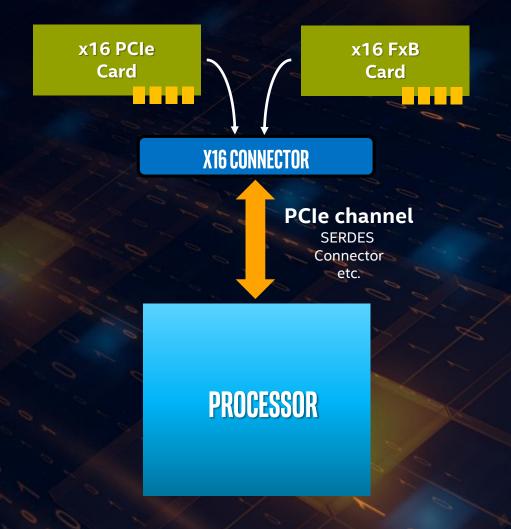


WHAT IS CXL?

• CXL is an alternate protocol that runs across the standard PCIe physical layer

• CXL uses a flexible processor port that can auto-negotiate to either the standard PCIe transaction protocol or the alternate CXL transaction protocols

- First generation CXL aligns to 32 Gbps PCIe Gen5
- CXL usages expected to be key driver for an aggressive timeline to PCIe Gen6

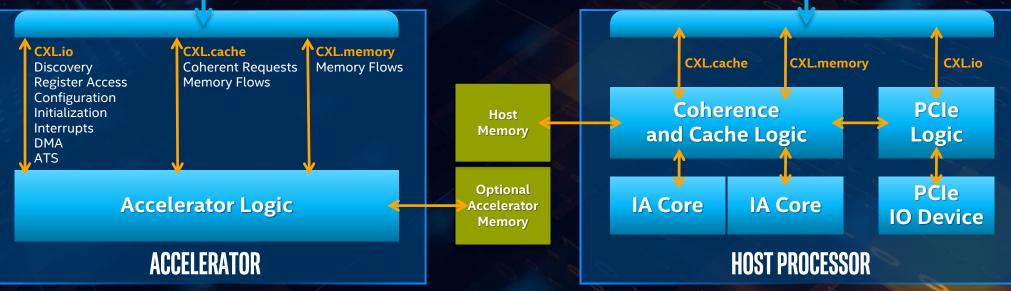




CXL PROTOCOLS

THE CXL TRANSACTION LAYER IS COMPRISED OF 3 DYNAMICALLY MULTIPLEXED SUB-PROTOCOLS ON A SINGLE LINK:

- CXL.io Discovery, configuration, register access, interrupts, etc.
- CXL.cache Device access to processor memory
- CXL.memory Processor access to device attached memory

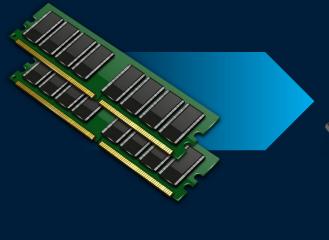


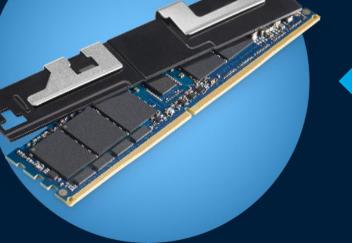
CXL-DYNAMICALLY MULTIPLEXED IO, CACHE AND MEMORY



INTRODUCING INTEL[®] OPTANE[™] DC PERSISTENT MEMORY









ENHANCE DATA INSIGHTS BY REDEFINING THE MEMORY AND STORAGE HIERARCHY

SIZE AND DATA PERSISTENCE OF STORAGE

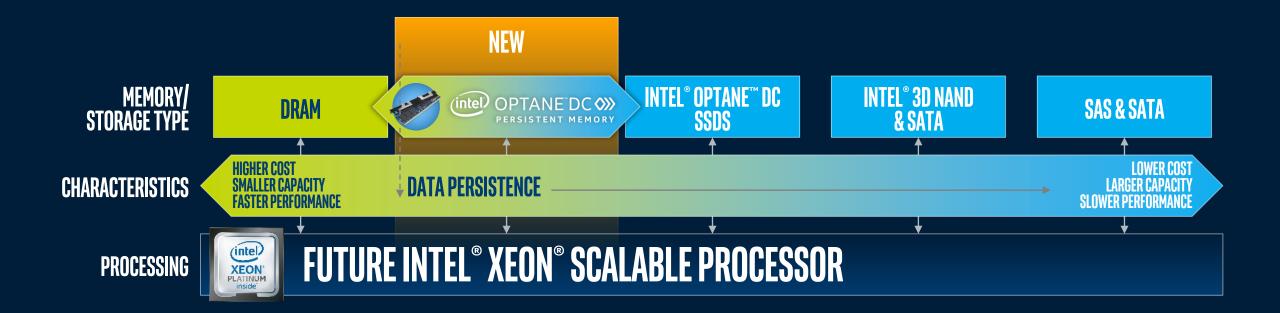
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Supported on future Intel[®] Xeon[®] Scalable Processors Platinum and Gold SKUs





REDEFINING THE MEMORY AND STORAGE HIERARCHY



PERFORMANCE OF MEMORY, PERSISTENCE OF STORAGE. FLEXIBLE AND SCALABLE TO ACCELERATE YOUR DATA INSIGHTS.



OPERATING MODES

"APP DIRECT" MODE APP/WORKLOAD DIRECT ACCESS TO HIGH SPEED, HIGH CAPACITY STORAGE



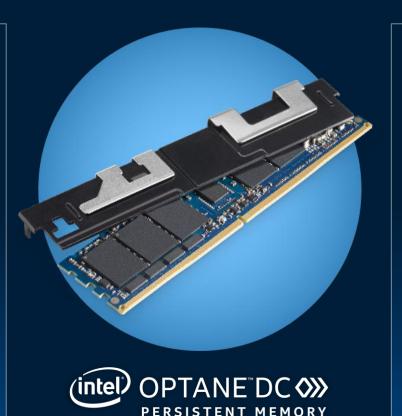




High availability/ less downtime



Significantly faster storage



MEMORY MODE Platform/os/App access to High speed, High capacity memory



High capacity Targeting >1.2X More VMs¹



Affordable capacity 128GB, 256GB and 512GB Modules

Ease of adoption No code changes required

BUILT-IN FLEXIBILITY TO USE BOTH MODES SIMULTANEOUSLY

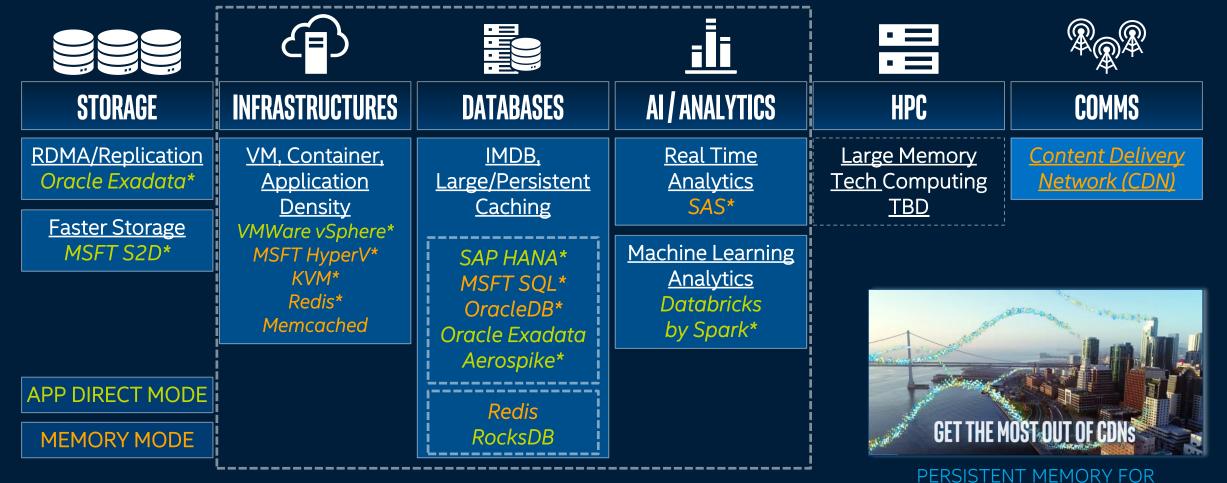
Performance results are based on testing as of dates shown in configuration and may not reflect all publicly available security updates. See configuration disclosure for details. No product or component can be absolutely secure. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.



Target List as of 04/02/2019

INTEL[®] OPTANE[™] DC PERSISTENT MEMORY TARGET WORKLOADS WITH APPLICATION SUPPORT FOR LAUNCH





REVENUE-FOCUSED + HIGHEST AEP AFFINITY

*Other names and brands may be claimed as the property of others.



SEAMLESS CONTENT DELIVERY



ECOSYSTEM SUPPORT



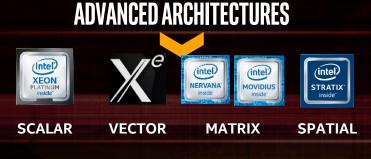


DEVELOPER RESOURCES FOR INTEL® OPTANE™ DC PERSISTENT MEMORY

Find the PMDK (Persistent Memory Development Kit) at http://pmem.io/pmdk/	 Getting Started Intel IDZ persistent memory- https://software.intel.com/en-us/persistent- memory Entry into overall architecture - http://pmem.io/2014/08/27/crawl-walk- run.html Emulate persistent memory - http://pmem.io/2016/02/22/pm- emulation.html 	Persistent Memory Programming Video Series - <u>https://software.intel.com/en-us/persistent-memory/get-started/series</u>
 Linux Resources Linux* Community Pmem Wiki - <u>https://nvdimm.wiki.kernel.org/</u> Pmem enabling in SUSE Linux Enterprise 12 SP2 - <u>https://www.suse.com/communities/blog/n</u> <u>vdimm-enabling-suse-linux-enterprise-12-</u> <u>service-pack-2/</u> 	 Windows* Resources Using Byte-Addressable Storage in Windows Server 2016 - <u>https://channel9.msdn.com/Events/Build/2</u> 016/P470 Accelerating SQL Server 2016 using Pmem <u>https://channel9.msdn.com/Shows/Data- Exposed/SQL-Server-2016-and-Windows- Server-2016-SCMFAST</u> 	 Other Resources SNIA Persistent Memory Summit 2018 - <u>https://www.snia.org/pm-summit</u> Intel manageability tools for Pmem - <u>https://01.org/ixpdimm-sw/</u>



FOCUSED INVESTMENTS TO ACCELERATE HPC & AI



+ Quantum & Neuromorphic

COMPUTE ARCHITECTURES FOR ALL YOUR WORKLOADS





UNIFIED SINGLE SOFTWARE ABSTRACTION AND DOMAIN-SPECIFIC LIBRARIES



RE-ARCHITECTING THE MEMORY HIERARCHY AND FILE SYSTEMS

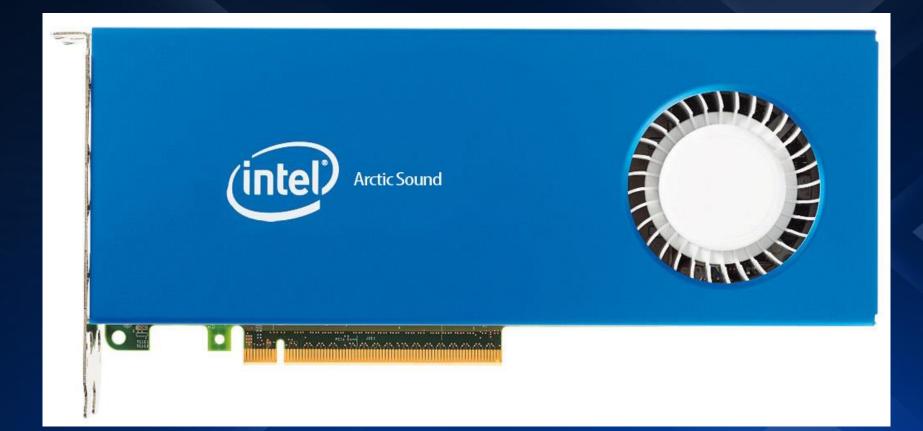


SECURITY AT ALL LEVELS: CORE, SOC, BOARD, PLATFORM, & SOFTWARE

UNIQUELY POSITIONED TO IMPLEMENT SECURITY TECHNOLOGIES AT EVERY LEVEL

GROWING THE ECOSYSTEM AND ADVANCING HPC & AI THROUGH OPEN STANDARDS







ACCELERATING AI

LEADERSHIP PERFORMANCE FOR DATA LEVEL PARALLEL AI WORKLOADS



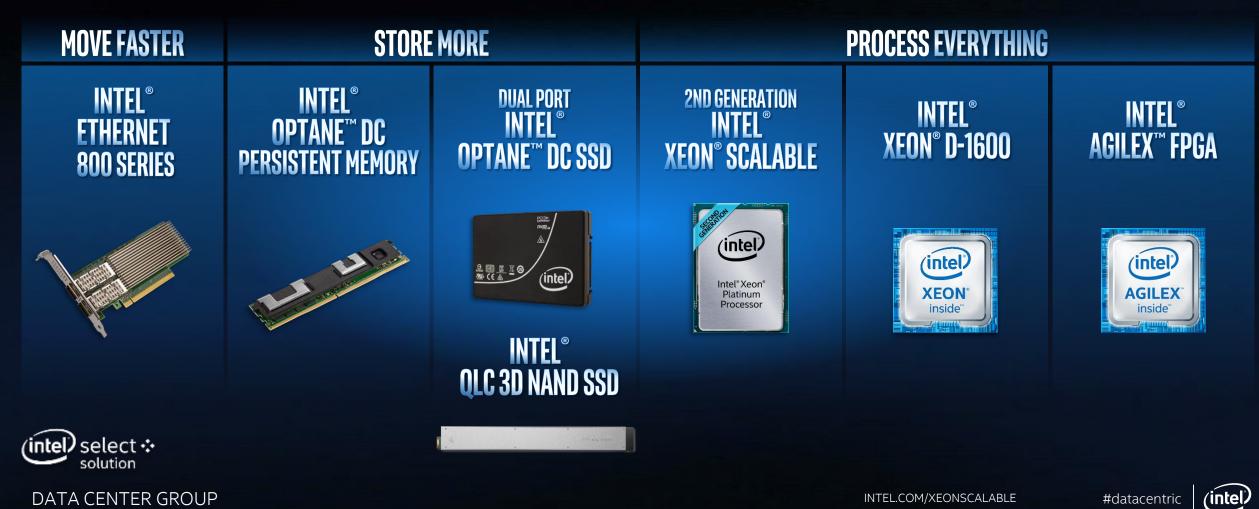
7NM PROCESS TECHNOLOGY

EMIB (2D) AND FOVEROS (3D) TECHNOLOGY

POVERNG AURORA DELIVERED IN 2021



ANNOUNCED ON APRIL 2, 2019 2019 DATA-CENTRIC PORTFOLIO



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ВОПРОСЫ?



